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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Yeo, *et al.* Docket No.: TSM03-0553
Serial No.: 10/667,871 Art Unit: 2811
Filed: September 22, 2003 Examiner: TBD
For: Resistor With Reduced Leakage

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Respectfully submitted,

Kristy Engeldahl

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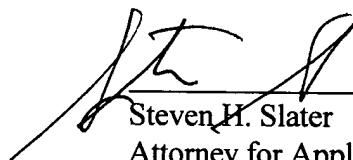
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The Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08A & 08B that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed pursuant to 37 C.F.R. § 1.97(b)(3), before the mailing of a first Office action on the merits. If any fee is required, please charge any additional amount, or credit any overpayment to Deposit Acct. No 50-1065 of the below mentioned firm..

Respectfully submitted,



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May 26, 2004

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Application Number	10/667,871
Sheet	2	of	3	Filing Date	September 22, 2003
				First Named Inventor	Yeo, et al.
				Group Art Unit	2811
				Examiner Name	TBD
				Attorney Docket Number	TSM03-0553

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS						
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.				T ²
	23	ISMAIL, K., et al., "Electron Transport Properties of Si/SiGe Heterostructures: Measurements and Device Implications," Applied Physics Letters, Vol. 63, No. 5, (August 2, 1993), pp. 660-662.				
	24	NAYAK, D.K., et al., "Enhancement-Mode Quantum-Well Ge _x Si _{1-x} PMOS," IEEE Electron Device Letters, Vol. 12, No. 4, (April 1991), pp. 154-156.				
	25	GÁMIZ, F., et al., "Strained-Si/SiGe-on-Insulator Inversion Layers: The Role of Strained-Si Layer Thickness on Electron Mobility," Applied Physics Letters, Vol. 80, No. 22, (June 3, 2002), pp. 4160-4162.				
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	27	MIZUNO, T., et al., "Novel SOI p-Channel MOSFETs With Higher Strain in Si Channel Using Double SiGe Heterostructures," IEEE Transactions on Electron Devices, Vol. 49, No. 1, (January 2002), pp. 7-14.				
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	32	TIWARI, S., et al., "Hole Mobility Improvement in Silicon-on-Insulator and Bulk Silicon Transistors Using Local Strain," International Electron Device Meeting, (1997), pp. 939-941.				
	33	OOTSUKA, F., et al., "A Highly Dense, High-Performance 130nm Node CMOS Technology for Large Scale System-on-a-Chip Applications," International Electron Device Meeting, (2000), pp. 575-578.				
	34	MATTHEWS, J.W., et al., "Defects in Epitaxial Multilayers – I. Misfit Dislocations," Journal of Crystal Growth, Vol. 27, (1974), pp. 118-125.				
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Examiner Signature					Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	36	MATTHEWS, J.W., et al., "Defects in Epitaxial Multilayers – III. Preparation of Almost Perfect Multilayers," <i>Journal of Crystal Growth</i> , Vol. 32, (1976), pp. 265-273.		
	37	SCHÜPPEN, A., et al., "Mesa and Planar SiGe-HBTs on MBE-Wafers," <i>Journal of Materials Science: Materials in Electronics</i> , Vol. 6, (1995), pp. 298-305.		
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	39	HUANG, X., et al., "Sub-50 nm P-Channel FinFET," <i>IEEE Transactions on Electron Devices</i> , Vol. 48, No. 5, May 2001, pp. 880-886.		
	40	SHAHIDI, G.G., "SOI Technology for the GHz Era," <i>IBM J. Res. & Dev.</i> , Vol. 46, No. 2/3, March/May 2002, pp. 121-131.		
	41	SHIMIZU, A., et al., "Local Mechanical Stress Control (LMC): A New Technique for CMOS-Performance Enhancement," <i>IEDM</i> 2001, pp. 433-436.		
	42	WONG, H.-S.P., "Beyond the Conventional Transistor," <i>IBM J. Res. & Dev.</i> , Vol. 46, No. 2/3, March/May 2002, pp. 133-167.		
	43	YANG, F.L., et al., "25 nm CMOS Omega FETs," <i>IEDM</i> 2002, pp. 255-258.		
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	46	WELSER, J., et al., "NMOS and PMOS Transistors Fabricated in Strained Silicon/Relaxed Silicon-Germanium Structures," <i>IEDM</i> 1992, pp. 1000-1002.		
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